Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **VIN**
2. **VOUT**
3. **VIN**
4. **VIN**
5. **VOUT**
6. **VOUT SENSE**
7. **ADJ**
8. **N/C**
9. **VIN**
10. **VOUT**
11. **VOUT**

**.121”**

**1083**

**MASK**

**REF**

**2 11**

**5 10**

**1**

**3**

**4**

**9**

**6**

**7**

**8**

**.160”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size = .004 x .004” min.**

**Backside Potential: VOUT**

**Mask Ref: 1083**

**APPROVED BY: DK DIE SIZE .121” X .160” DATE: 6/29/23**

**MFG: LINEAR TECH THICKNESS .012” P/N: LT1083**

**DG 10.1.2**

#### Rev B, 7/1